AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A video controller raster engine that receives video data from a frame buffer and renders formatted data to a display in a computer system, the raster engine comprising:

a first in first out (FIFO) memory that interfaces a host bus in the computer system with the raster engine and obtains video data from the frame buffer via the host bus to provide video data to a video pipeline;

a first input counter that has a first input counter value indicative of video data obtained from the frame buffer;

a first output counter that has a first output counter value indicative of video data provided to the video pipeline; and

a control logic system, associated with the FIFO memory, that provides an underflow indication according to the first input and output counter values.

2. (Original) The raster engine of claim 1, wherein the underflow indication comprises an underflow signal indicating at least one of an existing underflow condition, an anticipated underflow condition, and a raster engine lockup condition.

3. (Previously Presented) The raster engine of claim 2, wherein the control logic system provides the underflow signal to a host processor in the computer system.

4. (Original) The raster engine of claim 2, wherein the underflow signal indicates one of an existing underflow condition and an anticipated underflow condition when the first input and output counter values are within a threshold value of each other.

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5. (Previously Presented) The raster engine of claim 4, wherein the raster engine comprises an underflow threshold value register programmable by a host processor in the computer system, and wherein the control logic system obtains the threshold value from the threshold value register, and compares the threshold value with the difference between the first input and output counter values.

6. (Original) The raster engine of claim 4, wherein the underflow signal indicates an existing underflow condition when the first input and output counter values are equal, and an anticipated underflow condition when the first input and output counter values are within a threshold value of each other.

7. (Original) The raster engine of claim 6, wherein the FIFO memory obtains video data from the frame buffer according to a host clock and provides video data to the video pipeline according to a video clock, and wherein the underflow signal indicates an existing underflow condition when the first input and output counter values are equal for at least two cycles of the host clock, and an anticipated underflow condition when the first input and output counter values are within a threshold value of each other for at least two cycles of the host clock.

8. (Original) The raster engine of claim 1, wherein the control logic system comprises a first logic circuit adapted to subtract the first output counter value from the first input counter value to obtain a difference value, and wherein the control logic system provides an underflow indication if the comparison is less than or equal to a threshold value.

9. (Original) The raster engine of claim 8, wherein the control logic system comprises a second logic circuit adapted to compare the difference value with the threshold value.

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10. (Original) The raster engine of claim 8, wherein the FIFO memory obtains video data from the frame buffer according to a host clock and provides video data to the video pipeline according to a video clock, and wherein the control logic system provides an underflow indication if the comparison is less than or equal to a threshold value for at least two cycles of the host clock.

11. (Original) The raster engine of claim 1, wherein the FIFO memory obtains video data from the frame buffer according to a host clock and provides video data to the video pipeline according to a video clock, and wherein the control logic system provides the underflow indication when the first input and output counter values are equal for at least two cycles of the host clock, and when the first input and output counter values are within a threshold value of each other for at least two cycles of the host clock.

12. (Previously Presented) The raster engine of claim 1, further comprising:

a second input counter having a second input counter value indicative of video data obtained from the frame buffer; and

a second output counter having a second output counter value indicative of video data provided to the video pipeline;

wherein the raster engine selectively performs dual scan operation with the FIFO memory to provide interleaved first and second video data to the video pipeline represented by the first and second output counter values; and

wherein the control logic system provides an underflow indication according to the first input and output counter values and second input and output counter values.

13. (Original) The raster engine of claim 12, wherein the underflow indication comprises an underflow signal indicating at least one of an existing underflow condition, an anticipated underflow condition, and a raster engine lockup condition.

14. (Original) The raster engine of claim 13, wherein the underflow signal indicates one of an existing underflow condition and an anticipated underflow condition

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when the first input and output counter values are within a threshold value of each other or when the second input and output counter values are within the threshold value of each other.

15. (Previously Presented) The raster engine of claim 12, wherein the raster engine comprises an underflow threshold value register programmable by a host processor in the computer system, and wherein the control logic system obtains a threshold value from the threshold value register, and compares the threshold value with the difference between the first input and output counter values and with the difference between the second input and output counter values.

16. (Original) The raster engine of claim 12, wherein the FIFO memory obtains video data from the frame buffer according to a host clock and provides video data to the video pipeline according to a video clock, and wherein the control logic system provides the underflow indication when the first input and output counter values are equal for at least two cycles of the host clock, when the first input and output counter values are within a threshold value of each other for at least two cycles of the host clock, when the second input and output counter values are equal for at least two cycles of the host clock, and when the second input and output counter values are within a threshold value of each other for at least two cycles of the host clock.

17. (Previously Presented) A video underflow detection system that indicates an underflow condition in a video controller raster engine with a first in first out (FIFO) memory that interfaces a host bus and adapted to obtain video data from a frame buffer via the host bus and to provide video data to a video pipeline, the underflow detection system comprising:

a control logic system associated with the FIFO memory, a first input counter having a first input counter value indicative of video data obtained from the frame buffer, and a first output counter having a first output counter value indicative of video data provided to the video pipeline;

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wherein the control logic system provides an underflow indication according to the first input and output counter values.

18. (Original) The underflow detection system of claim 17, wherein the underflow indication comprises an underflow signal indicating at least one of an existing underflow condition, an anticipated underflow condition, and a raster engine lockup condition.

19. (Original) The underflow detection system of claim 18, wherein the underflow signal indicates one of an existing underflow condition and an anticipated underflow condition when the first input and output counter values are within a threshold value of each other.

20. (Original) The underflow detection system of claim 19, wherein the underflow signal indicates an existing underflow condition when the first input and output counter values are equal, and an anticipated underflow condition when the first input and output counter values are within a threshold value of each other.

21. (Original) The underflow detection system of claim 20, wherein the FIFO memory obtains video data from the frame buffer according to a host clock and provides video data to the video pipeline according to a video clock, and wherein the underflow signal indicates an existing underflow condition when the first input and output counter values are equal for at least two cycles of the host clock, and an anticipated underflow condition when the first input and output counter values are within a threshold value of each other for at least two cycles of the host clock.

22. (Previously Presented) The underflow detection system of claim 17, wherein the control logic system comprises a first logic circuit that subtracts the first output counter value from the first input counter value to obtain a difference value, and

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wherein the control logic system provides an underflow indication if the comparison is less than or equal to a threshold value.

23. (Previously Presented) The underflow detection system of claim 22, wherein the control logic system comprises a second logic circuit that compares the difference value with the threshold value.

24. (Original) The underflow detection system of claim 22, wherein the FIFO memory obtains video data from the frame buffer according to a host clock and provides video data to the video pipeline according to a video clock, and wherein the control logic system provides an underflow indication if the comparison is less than or equal to a threshold value for at least two cycles of the host clock.

25. (Original) A method of detecting underflow conditions in a video controller raster engine, comprising:

obtaining an input counter value indicative of video data obtained from a frame buffer;

obtaining an output counter value indicative of video data provided from a memory to a video pipeline in the raster engine;

performing a comparison of the input and output counter values; and

selectively providing an underflow indication according to the input and output counter value comparison.

26. (Original) The method of claim 25, wherein selectively providing an underflow indication comprises providing an underflow signal if the input and output counter values are within a threshold value of each other.

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27. (Original) The method of claim 25, wherein performing a comparison of the input and output counter values comprises:

subtracting the output counter value from the input counter value to obtain a difference value; and

comparing the difference value with a threshold value.

28. (Original) The method of claim 27, wherein selectively providing an underflow indication comprises providing an underflow signal if the difference value is less than or equal to the threshold.

29. (Original) The method of claim 28, wherein the raster engine obtains video data from the frame buffer according to a host clock, and wherein selectively providing an underflow indication comprises providing an underflow signal if the difference value is less than or equal to the threshold for at least two cycles of the host clock.

30. (Previously Presented) A system for detecting underflow conditions in a video controller raster engine, comprising:

means for obtaining an input counter value indicative of video data obtained from a frame buffer;

means for obtaining an output counter value indicative of video data provided from a memory to a video pipeline in the raster engine;

means for performing a comparison of the input and output counter values; and

means for selectively providing an underflow indication according to the input and output counter value comparison.

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REMARKS

Claims 1-30 are currently pending in the subject application and are presently under consideration. A clean version of all pending claims is found at pages 2-8 of this Reply. No claims have been amended herein.

Applicant's representative thanks the Examiner for the courtesies extended during a telephonic interview on January 29, 2004. Although no agreement was reached during the interview vis-à-vis the subject claims, applicant's representative appreciates the Examiner's subsequent reconsideration of the subject claims and withdrawal of the previous rejection(s).

Favorable reconsideration of the subject patent application is respectfully requested in view of the comments herein.

I. Rejection of Claims 1-11, 17-30 Under 35 U.S.C. §103(a)

Claims 1-11, and 17-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Wang *et al.*, (U.S. 5,953,020) in view of Valmiki *et al.*, (U.S. 6,661,422), and further in view of Duzan (U.S. 5,214,607). This rejection should be withdrawn for at least the following reasons. Neither Wang *et al.* nor Valmiki *et al.* nor Duzan, alone or in combination, teach or suggest each and every aspect recited in the subject claims.

> To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP §706.02(j). The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *See In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

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The present invention relates to the field of video displays and more particularly to improved methods and apparatus for video underflow detection in a raster engine. Independent claim 1 recites, "*a control logic system associated with the FIFO memory and adapted to provide* ***an underflow indication according to the first input and output counter values.***" Independent claims 17, 25, and 30 recite similar aspects. "The raster engine comprises an underflow detection system, which may provide an *indication* of *current or anticipated underflow conditions*, which may be provided to a system processor or other device for taking some steps toward remedying the cause of the underflow." (Page 3, lines 13-16.) The raster engine of the claimed invention can "provide an *indication* to a host processor that the raster engine is *underflowing or about to underflow, or that a lockup condition exists* in the raster engine. Input and output counters in the raster engine first in first out (FIFO) memory system, which interface the host bus with the raster engine video systems, are read by an *underflow detection system* to provide an *underflow indication according to the counter values*. The underflow detection and indication system of the claimed invention minimizes or reduces undesirable visual effects associated with a starved or empty raster engine, and *allows remedial and/or notification measures to be taken in a computer system employing the raster engine.*" (*See e.g.*, page 3, lines 21-30.) Wang *et al.* does not teach or suggest providing an underflow *indication*, or that an underflow *indication* is based on FIFO counter values as in applicant's claimed invention.

The Examiner contends that Column 5, line 22-Column 6, line 66 of Wang *et al.* teaches a control logic system adapted to provide an underflow (and overflow) *indication*.

> A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

The Examiner relies on Column 5, lines 22-26: "...the virtual FIFO controller 68 serves as a virtual FIFO memory in the sense that an output (tDRAIN) generated from the programmable FIFO memory emulator 72 indicates the entry status of the actual display

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FIFO memory 70 from a fill and drain standpoint." However, Wang *et al.* states that the system described therein is structured so as to "*guarantee* that the display FIFO memory 70 *does not* overflow or *underflow*..." (*See* Column 6, lines 64-66.) *See also* Column 2, lines 26-29: "To *avoid* an underflow condition, an extra entry is typically added to the low watermark to compensate for the one clock re-synchronization uncertainty." Thus, like Kuchkuda *et al.*, cited in the previous office action, Wang *et al.* is designed to *prevent* an occurrence of underflow, such that providing an indication of underflow to permit remedial action and/or detection of a cause of underflow is not taught or suggested by Wang *et al.* Indeed, Wang *et al.* specifically mentions underflow only twice, and each occurrence thereof is with regard to preventing and avoiding underflow. Nowhere in the Examiner's cited sections or otherwise does Wang *et al.* suggest providing an indication that underflow is occurring, is imminent, *etc.* Furthermore, Wang *et al.* is incapable of providing an underflow indication because underflow is not permitted to occur.

Still furthermore, "the display FIFO emulator 72 continually shows how many memory clocks are left over before the display FIFO memory 70 needs refilling, *without using read and write pointer comparison methods*." (Column 6, lines 41-44.) Thus, Wang *et al.* actually *teaches away* from the present invention as set forth in the subject independent claims, which recite comparing input and output values to provide an underflow indication.

Valmiki *et al.* fails to overcome the aforementioned deficiencies of Wang *et al.* Valmiki *et al.* discloses a system for processing compressed video data. Nothing in Valmiki *et al.* suggests that the system described therein is capable of *providing an underflow indication*, let alone providing an underflow indication according to the first input and output counter values as in applicant's invention as recited in the subject claims.

> A reference that teaches away from another reference may not be combined there with to form the basis of a 35 U.S.C. §103 rejection. (*See, e.g., In Re Grasselli*, 713 F.2d 731, 218 USPQ 769, 779, Fed. Cir. 1983; "It is improper to combine references where the references teach away from their combination.")

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Duzan similarly fails to overcome the deficiencies of Wang *et al.* with respect to the subject claims. Specifically, Duzan does not teach or suggest providing an indication of underflow, whether impending or extant. Moreover, the Examiner relies on Duzan to teach first input and output counters that facilitate providing an underflow indication. As stated above, Wang *et al.* teaches away from employing read and write pointer comparison methods. Accordingly, Wang *et al.* and Duzan cannot properly be combined to form the basis of a rejection under 35 U.S.C. §103(a).

Furthermore, the non-obviousness applicant's claimed invention is additionally supported by multiplicity of references cited by the Examiner. In addition, the mere fact that references can be modified does not render the modification obvious unless the cited art also suggests the desirability of the modification. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). It appears the Examiner is impermissibly employing 20/20 hindsight with applicants' specification as a roadmap to make the purported combination. The rationale proffered to modify and combineWang *et al.*, Valmiki *et al.*, and/or Duzan is to achieve benefits identified in applicant's specification, which overcome problems associated with conventional systems and/or methods. Applicant's representative respectfully submits that this is an unacceptable and improper basis for a rejection under 35 U.S.C. §103. In essence, the Examiner is basing the rejection on the assertion that it would have been obvious to do something not suggested in the art because so doing would provide advantages stated in applicants' specification. This sort of rationale has been condemned by the Court of Appeals for the Federal Circuit. *See, for example, Panduit Corp. v. Dennison Manufacturing Co.*, 1 USPQ2d 1593 (Fed. Cir. 1987).

In view of the above, it is readily apparent that neither Wang *et al.* nor Valmiki *et al.* nor Duzan, alone or in combination, make obvious applicant's invention as recited in independent claims 1, 17 and 25 (and claims 2-11, 18-24, and 26-29, which depend respectively there from). Therefore, this rejection should be withdrawn.

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II. **Rejection of Claims 12-16 Under 35 U.S.C. §103(a)**

Claims 12-16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Wang *et al.*, (U.S. 5,953,020) in view of Valmiki *et al.*, (U.S. 6,661,422), and further in view of Duzan (U.S. 5,214,607) as applied to claim 1 above, and further in view of Rudin *et al.*, U.S. (5,959,640) and Reddy, (U.S. 6,195,079). This rejection should be withdrawn for at least the following reasons. Claims 12-16 depend from independent claim 1 -- in view of at least the above comments, the subject invention as recited in these dependent claims is not made obvious by Wang *et al.*, Valmiki *et al.*, and/or Duzan, alone or in combination.

Neither Rudin *et al.* nor Reddy overcome the deficiencies of Wang *et al.*, Valmiki *et al.*, and Duzan with respect to independent claim 1. Specifically, neither reference teaches or suggests "*a control logic system associated with the FIFO memory that provides an underflow indication according to the first input and output counter values.*" Therefore, this rejection should be withdrawn.

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CONCLUSION

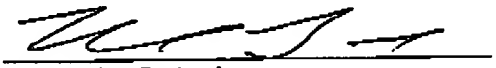
The present application is believed to be in condition for allowance in view of the above comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063.

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

AMIN & TUROCY, LLP



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